Search Program

Case under review	Patent found	Noteable comment:
8,798,227	5,488,325	time delay generator
Class:	326 / 93	
8,798,227	5,587,672	suspendable clock
Class:	326 / 93	
8,798,227	5,608,343	bias change fetching input synchronize
Class:	326 / 93	
8,798,227	5,625,311	phase system clock generation circuit
Class:	326 / 93	
8,798,227	5,635,857	matching path delays, providing accurately timed signals
Class:	326 / 93	
8,798,227	5,793,233	phase detection logic pipeline
Class:	326 / 93	
8,798,227	5,801,562	detects a phase difference between clock signals
Class:	326 / 93	
8,798,227	5,812,462	skewed transitions
Class:	326 / 93	
8,798,227	5,857,005	Multiple clocks to synchronize memory data translaters.
Class:	326 / 93	
8,798,227	5,880,607	multiple level clock distribution.
Class:	326 / 93	
8,798,227	5,880,608	domino evaluation tree
Class:	326 / 93	
8,798,227	5,867,692	synchronize delay
Class:	395 / 551	
8,798,227	5,872,903	restarting clock signals
Class:	395 / 551	
8,798,227	5,875,354	clocks with modified rates of operation
Class:	395 / 551	
8,798,227	2,945,213	Delay means.
Class:	711 / 100	
8,798,227	2,993,195	Clock generator and delay.
Class:	711 / 100	
8,798,227	2,994,065	Synchronized storage.
Class:	711 / 100	
8,798,227	4,011,556	Command timing signals, pattern generation.
Class:	711 / 100	
8,798,227	4,376,974	Offset comparator.
Class:	711 / 100	
8,798,227	4,639,890	Phase matching to multiple sources.
Class:	711 / 100	
8,798,227	4,924,426	Create timing from sync signal.
Class:	711 / 100	

Search Program

Case under review	Patent found	Noteable comment:
8,798,227	5,784,704	Memory timer.
Class:	711 / 100	
8,798,227	5,819,076	propogation delay; output gate; dynamic delay states
Class:	711 / 100	
8,798,227	5,819,305	differential operating mode
Class:	711 / 100	
8,798,227	5,825,706	timing delay addressed; DRAM controller
Class:	711 / 100	
8,798,227	5,850,509	test mode
Class:	711 / 100	
8,798,227	5,857,095	prog. Delay; output gate
Class:	711 / 100	
8,798,227	4,167,782	Delay line.
Class:	711 / 141	
8,798,227	5,398,325	Snooping request; request; reply.
Class:	711 / 141	
8,798,227	5,466,504	Time differencess in clocking frequencies.
Class:	711 / 141	
8,798,227	5,481,731	Phase generators from delay phase locked loops.
Class:	711 / 141	
8,798,227	5,530,932	Phased locked loop; internal clock; snoop.
Class:	711 / 141	
8,798,227	5,608,878	Multiple IO bus.
Class:	711 / 141	
8,798,227	5,651,137	MESI Protocol.
Class:	711 / 141	
8,798,227	5,666,513	Multi-set tag RAM.
Class:	711 / 141	
8,798,227	5,673,413	Multi-nodal requestor; respondandt coherency.
Class:	711 / 141	
8,798,227	5,740,448	Clock synthysis circuit.
Class:	711 / 141	
8,798,227	5,781,757	Snoop in; snoop out.
Class:	711 / 141	
8,798,227	5,699,548	Write through with synchronizer.
Class:	711 / 142	
8,798,227	5,732,748	Wait state.
Class:	711 / 142	
8,798,227	5,737,748	Suspended clock.
Class:	711 / 142	
8,798,227	5,768,558	Write back cycle.
Class:	711 / 142	

Search Program

Case under review	Patent found	Noteable comment:
8,798,227	5,778,425	Timer counter; interrupt control; writeback.
Class:	711 / 142	
8,798,227	5,832,276	delay and acknowledge
Class:	711 / 146	
8,798,227	5,794,054	halting the clock; self test
Class:	711 / 147	
8,798,227	3,368,203	Checking system, delay line synchronization.
Class:	711 / 167	
8,798,227	3,377,621	Phase counters.
Class:	711 / 167	
8,798,227	3,417,378	Timing and control.
Class:	711 / 167	
8,798,227	3,493,936	Controller with memory and logic circuit, timing and delay.
Class:	711 / 167	
8,798,227	3,629,846	Time slot delay storage, multi-phase.
Class:	711 / 167	
8,798,227	4,270,185	Synchronizer for transmitter and receiver.
Class:	711 / 167	
8,798,227	4,288,860	FIFO Buffer, assynchronous clock, speed change.
Class:	711 / 167	
8,798,227	5,408,639	Multiple clocks system.
Class:	711 / 167	
8,798,227	5,522,067	Phased locked loop.
Class:	711 / 167	
8,798,227	5,652,733	Multiphase delayed clock.
Class:	711 / 167	
8,798,227	5,684,973	Multibank, delay line DRAM.
Class:	711 / 167	
8,798,227	5,752,267	PA first set bits; second set of bits; timing.
Class:	711 / 167	
8,798,227	5,778,445	Request and acknowledge.
Class:	711 / 167	

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Patent Search III

(FILE 'USPAT' ENTERED AT 09:55:11 ON 26 MAR 1999)
SET HIGHLIGHT OFF

L1	30073	S	(326 OR 395 OR 711)/CLAS
L2	21342	S	L1 AND MEMORY
L3	11239	S	L1 AND CLOCK
L4	4	S	L1 AND DELAY LOCKED LOOP
L5	12330	S	L1 AND (DELAY OR PHASE)
L6	9810	S	L1 AND CONTROLLER
L7	14	S	L1 AND VERNIER
L8	3	S	L2 AND L3 AND L4 AND L6
L9	3	S	L8 AND PHASE
L10	0	S	L9 AND L7
L11	0	S	L4 AND L7
L12	1	S	L2 AND L3 AND L5 AND L6 AND L7
L13	2946	S	L2 AND L3 AND L5 AND [illegible]
L14	1615	S	L13 AND CLOCK (P) (DELAY OR PHASE)
L15	1109	S	L13 AND DELAY (P) MEMORY
L16	3	S	L13 AND MEMORY (P) CONTROLER
L17	1445	S	L13 AND CONTROLLER (P) CLOCK
L18	371	S	L13 AND CONTROLLER (P) CLOCK (P) (PHASE OR DELAY)
L19	10	S	L13 AND ECHO (P) CLOCK
L20	2	S	L14 AND L15 AND L16 AND L19
L21	0	S	L19 AND L20
L22	2	S	L16 AND L20
L23	0	S	L4 AND L19
L24	0	S	L4 AND ECHO (P) CLOCK
L25	4	S	L4 AND PHASE (P) DELAY
L26	3	S	L25 AND MEMORY

Patent

US PAT NO: 5,845,108 [IMAGE AVA... L9: 1 of 3
TITLE: Semiconductor memory ... ...g asynchronous signal

US PAT NO: 5,805,873 [IMAGE AVA... L9: 2 of 3
TITLE: Phase linking of outp... ...h master clock in memory architecture

US PAT NO: 5,754,838 [IMAGE AVA... L9: 3 of 3
TITLE: Synchronous dynamic ... ...ce capable of operating over wide range of ... frequenci...

US PAT NO: 5,517,626 [IMAGE AV... L22: 1 of 2
TITLE: Open high speed bus ... ...puter system

US PAT NO: 4,425,616 [IMA... ...: 2 of 2
TITLE: High-speed time ...

US PAT NO: 5,845,108 [IMAGE ... ...6: 1 of 3
TITLE: Semiconductor ... ...g asynchronous signal

US PAT NO: 5,805,873 [IMA... ...: 2 of 3
TITLE: Phase linking of ... ...h ... clock in memory architecture

US PAT NO: 5,754,838 [IMAGE AV... ...26: 3 of 3
TITLE: Synchronous dynam... ... capab... of operating over wide range ... frequenci...